METHOD OF FABRICATING COPPER DAMASCENE AND DUAL DAMASCENE INTERCONNECT WIRING

DESCRIPTION

[Para 1] FIELD OF THE INVENTION

[Para 2] The present invention relates to the field of integrated circuit fabrication; more specifically, it relates to method of fabricating copper damascene and dual damascene wires.

[Para 3] BACKGROUND OF THE INVENTION

[Para 4] Semiconductor manufacturers must contend with continually decreasing device sizes, wire widths and wire thicknesses and power consumption as well as increasing device density, wire density and operating frequencies. These requirements have led the semiconductor industry to utilize copper wiring in place of older wire materials, for example,

those based on aluminum and aluminum alloys. For example, aluminum has problems associated with heat dissipation and electro-migration. Copper, which has a lower resistivity and greater electro-migration lifetime eliminates many of the problems associated with aluminum and is more suitable for use in low-power, low-voltage and high speed applications. However, there are difficulties with fabricating copper interconnects because copper is more reactive than aluminum and can diffuse through many dielectric materials complicating the fabrication process of copper wiring. Therefore, there is a need for a method of fabricating copper interconnect wiring that reduces the risk of problems related to the reactivity of copper and the diffusion of copper while still providing a cost effective manufacturable process.

[Para 5] SUMMARY OF THE INVENTION

[Para 6] A first aspect of the present invention is a method of manufacturing an interconnect, comprising: (a) providing a substrate; (b) forming a dielectric layer on the substrate; (c) forming a wire in the dielectric layer, a top surface of the wire coplanar with a top surface of the dielectric layer; (d) forming a first capping layer on the top surface of the wire and the top surface of the dielectric layer, the first capping layer thin enough to allow penetration of the first capping layer by a point of a conductive probe tip in order to

make electrical contact to the wire; and (e) after step (d) forming a second capping layer on a top surface of the first capping layer.

[Para 7] A second aspect of the present invention is a method of manufacturing an integrated circuit, comprising: (a) providing a substrate; (b) forming a copper diffusion barrier layer on the substrate; (c) forming a dielectric layer on a top surface of the copper diffusion barrier layer; (d) forming a copper damascene or dual damascene wire in the dielectric layer, a top surface of the copper damascene or dual damascene wire coplanar with a top surface of the dielectric layer; (e) forming a first capping layer on the top surface of the wire and the top surface of the dielectric layer; (f) after step (e) performing one or more characterization procedures in relation to the integrated circuit; and (g) after step (f) forming a second capping layer on the top surface of the first capping layer.

[Para 8] A third aspect of the present invention is an integrated circuit, comprising: a copper damascene or dual damascene wire in a fluorinated silicon glass dielectric layer, a top surface of the copper damascene or dual damascene wire coplanar with a top surface of the fluorinated silicon glass dielectric layer; a first capping layer formed on the top surface of the copper damascene or dual damascene wire and the top surface of the fluorinated silicon glass dielectric layer; and a second capping layer formed on the top surface of the first

capping layer, the first capping layer thin enough to allow performance of one or more characterization procedures in relation to the integrated circuit and thick enough to prevent formation, on the top surface of the copper damascene or dual damascene wire, of copper containing particles by reaction of copper in the copper damascene or dual damascene wire with fluorine in the fluorinated silicon glass dielectric layer.

[Para 9] A fourth aspect of the present invention is a method of manufacturing an interconnect, comprising: (a) providing a substrate; (b) forming a copper wire in a dielectric layer, the dielectric layer having a top surface; (c) exposing a copper top surface of the copper wire, the copper top surface of the copper wire coplanar with the top surface of the dielectric layer or exposing the copper top surface of the copper wire in a bottom of a trench formed in the dielectric layer; after step (c), (d) storing the substrate in a controlled environment; and after step (d), (e) performing further processing steps on the substrate.

[Para 10] A fifth aspect of the present invention is a method of manufacturing an interconnect, comprising: (a) providing a substrate; (b) forming a copper wire in a dielectric layer, the dielectric layer having a top surface; (c) exposing a copper top surface of the copper wire, the copper top surface of the copper wire coplanar with the top surface of the dielectric layer or exposing the copper top surface of the copper wire in a bottom of a trench formed in the dielectric

layer to an ambient atmosphere for a period of time; after step (c), (d) if the period of time exceeds a predetermined period of time, performing a rework clean or a rework chemical mechanical polish; and after step (d), (e) performing further processing steps on the substrate.

[Para 11] BRIEF DESCRIPTION OF DRAWINGS

[Para 12] The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

[Para 13] FIG. 1 is a partial cross-sectional view illustrating a typical damascene copper interconnect;

[Para 14] FIGs. 2A and 2B are a partial cross-sectional views illustrating a newly discovered corrosion problems associated with the exposed copper interconnect wiring of FIG. 1;

[Para 15] FIGs. 3A through 3I are partial cross-sectional views of a method of fabricating copper interconnect wires according to a first embodiment of the present invention;

[Para 16] FIGs. 4A and 4B are partial cross-sectional views of a method of fabricating copper interconnect wires

according to a second embodiment of the present invention; and

[Para 17] FIG. 5 is a flowchart of the method of fabricating copper interconnect wires according to the present invention.

[Para 18] DETAILED DESCRIPTION OF THE INVENTION

[Para 19] A damascene process is one in which wire trench or via openings are formed in a dielectric layer, an electrical conductor deposited on a top surface of the dielectric of sufficient thickness to fill the trenches and a chemical-mechanical-polish (CMP) process performed to remove excess conductor and make the surface of the conductor co-planer with the surface of the dielectric layer to form a damascene wires (or damascene vias).

[Para 20] A dual damascene process is one in which via openings are formed through the entire thickness of a dielectric layer followed by formation of trenches part of the way through the dielectric layer in any given cross-sectional view. All via openings are intersected by integral wire trenches above and by a wire trench below, but not all trenches need intersect a via opening. An electrical conductor is deposited on a top surface of the dielectric of sufficient thickness to fill

the trenches and via opening and a CMP process performed to make the surface of the conductor in the trench co-planer with the surface the dielectric layer to form dual damascene wire and dual damascene wires having integral dual damascene vias. A dual damascene wire is thus a special case of a damascene wire. In an alternative dual damascene process sequence, the wire trenches are formed before the via openings.

[Para 21] In both damascene and dual damascene processes the deposited electrical conductor may include one or more thin conductive liner layers and a thicker core conductor layer.

[Para 22] FIG. 1 is a partial cross-sectional view illustrating a typical damascene copper interconnect. In FIG. 1, formed on a substrate 100 is a wiring level 105. Wiring level 105 includes a dielectric copper diffusion barrier layer 110 and an interlevel dielectric (ILD) layer 115 formed on a top layer surface 120 of dielectric copper diffusion barrier 110. Formed in ILD layer 115 are wires 125. A dielectric copper diffusion barrier layer is defined as a layer comprising a dielectric material of sufficient thickness to block the diffusion of copper species through the layer over the expected lifetime and operating voltages and temperature of the integrated circuit chip in which it is incorporated. Top surfaces 130 of wires 125 are substantially coplanar with a top surface 135 of ILD layer 115. Wires 125 comprise an inner liner 140, an optional outer

liner 145 and a copper core conductor 150. Wires 125 may be damascene or dual damascene wires. In one example, inner liner 140 comprises tantalum (Ta), outer liner 145 comprises tantalum nitride (TaN) and dielectric copper diffusion barrier 110 comprises silicon nitride (Si_xN_y). Of particular interest to the present invention is when ILD layer 115 comprises a dielectric which may be reactive with core conductor 150, such as fluorinated silicon oxide ($Si_xO_yF_z$) also called fluorinated silicon glass (FSG). It should be noted that wiring level 105 is exemplary of any one many wiring levels used in integrated circuits and there may be additional wiring levels in substrate 100 below wiring level 105.

[Para 23] FIGs. 2A and 2B are a partial cross-sectional views illustrating a newly discovered corrosion and particulate growth problems associated with the exposed copper interconnect wiring of FIG. 1. In FIG. 2A, the structures illustrated in FIG. 1 have been allowed to sit exposed to ambient atmosphere air. It can be seen that particles 155 which have been found to comprise copper oxy-fluoride ($Cu_xO_yF_z$) have formed on the exposed copper of top surfaces 130 of wires 125 and may bridge between wires 125 as shown. Growth and nucleation of particles 155 to a size sufficient to bridge between two adjacent wires 125 is a function of time, the distance between wires 125, moisture content and temperature of the air and the fluorine content of ILD layer 115.

[Para 24] Exposure to ambient air comes about during the normal inline probing and testing, measurement and inspection procedures carried out during the manufacture of integrated circuits.

[Para 25] While $Cu_xO_yF_z$ may itself be non-conductive, subsequent processing (for example. cleaning in ammonia, hydrogen or other reducing chemical) steps prior to formation upper wiring levels, chemically reduces the $Cu_xO_yF_z$ to Cu which is conductive and may short adjacent wires 125 together.

[Para 26] In FIG. 2B, formed on top surface 135 of ILD layer 115 is a level 160. Level 160 includes a dielectric copper diffusion barrier layer 165 and an interlevel ILD layer 170 formed on top layer surface 120 of dielectric copper diffusion barrier 165. Formed through ILD layer 170 and dielectric copper diffusion barrier layer 165 is a wire trench/via opening 175 exposing top surface 130 of wire 125.

[Para 27] In FIG. 2B, the exposed top surface 130 of wire 125 has been allowed to sit exposed to ambient air. It can be seen that particles 156 have formed on the exposed copper of top surfaces 130 of wires 125. Particles 156 may be, for example, comprised of $Cu_xO_yF_x$ as described *supra*, or $N_xH_yF_z$. When wire trench/via opening 175 is filled with metallurgy (such as a Ta liner and copper core similar to that described *supra* for wire 125) particles 156 or their residue after an

optional degas, plasma and/or sputter clean performed prior to liner deposition, will increase the resistance of the via and or wire formed in wire trench/via opening 175.

[Para 28] Exposure to ambient air in this case comes about because of normal process queuing as well as inline inspections and testing.

[Para 29] FIGs. 3A through 3I are partial cross-sectional views of a method of fabricating copper interconnect wires according to a first embodiment of the present invention. FIGs. 3A through 3I illustrate the present invention using a dual damascene process. The invention is equally applicable to single damascene processing where vias and studs are formed in adjacent levels to the wiring levels.

[Para 30] In FIG. 3A, formed on a substrate 200 is a dielectric copper diffusion barrier 205 and formed on a top surface 210 of dielectric copper diffusion barrier 205 is an ILD layer 215. In one example dielectric copper diffusion barrier layer 205 comprises Si_xN_y and is about 350 Å to about 900 Å thick. In one example, ILD layer 215 is FSG containing about 1% to about 9% fluorine by weight and is about 0.2 microns to about 6 microns thick. Formation of Si_xN_y by plasma-enhanced chemical-vapor-deposition (PECVD) is well known in the art. In a first example, FSG may be formed in a PECVD or high-density plasma CVD (HDPCVD) silane based process with the introduction of a fluorine containing gas such as SiF_4 into

the CVD chamber. In a second example, FSG may be formed in a PECVD or O_3 TEOS (tetraethoxysilane) based process with the introduction of a fluorine containing gas such as SiF_4 into the CVD chamber.

[Para 31] In FIG. 3B, a dual damascene wire trench 220 is formed in ILD layer 215 and a dual damascene wire trench 225 is formed in ILD layer 215 with a corresponding dual damascene via opening 230 formed in ILD layer 215 and dielectric copper diffusion barrier layer 205. Dual damascene wire trench 220, dual damascene wire trench 225 and dual damascene via 230 may be formed by one of any number of well known reactive ion etch (RIE) processes well known in the art. Dual damascene wire trenches 220 and 225 extend from a top surface 235 of ILD layer 215 part way toward dielectric copper diffusion barrier layer 205. Dual damascene via opening 230 extends from a bottom surface of dual damascene trench 225 through the entire remaining thickness of dielectric copper diffusion barrier 205 to substrate 200. Copper diffusion barrier layer 205 also acts as an RIE stop layer for ILD layer 215 etching.

[Para 32] In FIG. 3C, a conformal outer liner layer 240 is deposited on top surface of ILD layer 215 and all exposed surfaces of dual damascene wire trench 220, dual damascene wire trench 225, dual damascene via opening 230 and substrate 200 in the bottom of via opening 230. A conformal inner liner layer 245 is then deposited over all exposed

surfaces of outer liner layer 240. Then a conformal seed layer 250 is deposited over all exposed surfaces of inner liner layer 245. In one example, outer liner layer 240 comprises TaN and is about 50 Å to about 800 Å in thickness, inner liner layer 245 comprises Ta and is about 50 Å to about 800 Å in thickness and seed layer 250 comprises copper and is about 50 Å to about 700 Å in thickness. Alternatively outer liner layer 240, inner liner layer 245 and/or seed layer 250 may be formed by an evaporation process, an electroplating process or a sputtering process. Examples of deposition processes that may be used to form outer liner layer 240, inner liner layer 245 and seed layer 250 include but are not limited to physical vapor deposition (PVD), ionized PVD (IPVD), self ionized plasma (SIP) deposition, hollow cathode magnetron (HCM) deposition, CVD and atomic layer deposition (ALD).

[Para 33] In FIG. 3D, In particular, a thick copper layer 255 is formed over all exposed surfaces of seed layer 250. In one example, Cu electroplating is performed in a three step process consisting of: 1) low current plating initiation step; 2) medium current plating gap fill step; 3) high current plating overburden step. Step 3), the high current plating overburden step, has poor gap fill, and the medium current plating step 2) must be performed for enough time to completely fill dual damascene via opening 230 (see FIG. 3C). In one example, copper layer 255 has a thickness of about 0.5 microns to about 5 microns. In one example, copper layer 155 includes less than about 10 ppm to about 500 ppm by weight of compounds of carbon, compounds of chlorine, compounds

of nitrogen and compounds of sulfur, derived from additives added to the copper electro-plating solution.

[Para 34] In FIG. 3E, a CMP process is performed to form dual damascene wires 260 and dual damascene wire 265 with an integral dual damascene via 270 in ILD layer 215 and integral. An example of a suitable copper CMP process utilizes an aqueous Al_2O_3 or SiO_2 abrasive slurry containing $FeNO_3$ and possibly surfactants and copper passivating agents. Dual damascene wires 260 and 265 comprise an outer liner 275, an inner liner 280 and a copper core conductor 285. Top surfaces 290 of dual damascene wires 260 and 265 are substantially coplanar with a top surface 295 of ILD layer 215. Dual damascene wire 260 had a width W1 and a thickness D. Dual damascene wire 265 had a width W2 and a thickness D. Dual damascene wire 260 and dual damascene wire 265 are separated from one another by a space S. In one example W1 is between about 0.05 microns and about 10 microns, W2 is between about 0.05 microns and about 10 microns, D is between about 0.1 microns to about 1.2 microns and S is between about 0.05 microns and about 10 microns. In a second example W1 is greater than 10 microns. In a third example W2 is greater than 10 microns.

[Para 35] In FIG. 3F, a first capping layer 300 is deposited on all exposed surfaces of outer liner 275, inner liner 280, copper core conductor 285 and top surface 295 of ILD layer 215. Prior to deposition of first capping layer 300, a

cleaning operation may be performed to increase the adhesion of first capping layer 300 to copper core conductor 285. In one example, the cleaning process includes exposing copper core conductor 285 (as well as outer liner 275, inner liner 280 and top surface 295 of ILD layer 215) to ammonia, hydrogen or other reducing plasmas. In one example, first capping layer 300 comprises Si_xN_y, silicon carbide (Si_xC_y), silicon hydrogen carbide (SiC_xH_y), silicon oxy-nitride carbide ($SiC_xO_yN_z$) or silicon carbo-nitride (SiC_xN_y). In one example, first capping layer 300 is about 100 Å to about 300 Å thick. First capping layer 300 may be formed by high density plasma (HDP) or plasma enhanced CVD (PECVD) deposition.

[Para 36] In a first example, the thickness of first capping layer 300 is selected to be thin enough to allow characterization procedures such as optical microscopy and scanning electron microscopy (SEM) defect inspection and image size measurements of structures under the capping layer (i.e. thin enough to be transparent visible light and/or to back-scattered electrons in an SEM). In a second example, first capping layer 300 is thin enough to allow penetration of the capping layer by a probe tip during such characterization procedures as inline testing or parametric measurements. In all examples, first capping layer 300 is thick enough, however, to prevent formation of $Cu_xO_yF_z$ particles or Cu oxide, copper fluoride or other copper containing particles under the first

capping layer. However, first capping layer 300 may not be thick enough to act as a copper diffusion barrier.

[Para 37] FIG. 3G, illustrates that first capping layer 300 may be thin enough to allow a conductive probe tip 305 to penetrate through the first capping layer and make electrical contact with copper core conductor 285 during an inline test operation. At this time inline testing (i.e. electrical probing) may be performed to measure parametrics of transistors and other devices and interconnect wire and via structures for process control and yield projection. Optical and SEM defect inspection, such as that conducted for optical defect inspection or for optical or SEM mage size measurements and alignment may be performed at this time. Also, mask level alignment may be measured. Because of first capping layer 300 protecting copper core conductor 285, no time limit is required, nor are the wafers required to be an oxygen or water vapor controlled atmosphere.

[Para 38] In FIG. 3H, a second capping layer 310 is deposited on a top surface 315 of first capping layer 300. Prior to deposition of second capping layer 310 a cleaning operation may be performed to remove any debris generated by inline inspection, measurement or testing. In one example, the cleaning process cryogenic cleaning operation spraying cryogenic particles of CO_2, Ar or N_2 on top surface 315 of first capping layer 300. In addition, coating incoming particles with a thin dielectric layer may improve the cleaning efficiency. In